CLAIMS

Please amend the claims as follows:

1. (currently amended) A data processing system, comprising:

one or more processing cores; ~~and~~

a first memory controller, coupled to said one or more processing cores, that controls access to a first system memory containing a plurality of rows, said memory controller having an access history mechanism that maintains historical information regarding prior memory accesses, wherein said memory controller, responsive to a memory access request, directs an access to a selected row among the plurality of rows in the system memory to service the memory access request and speculatively causes the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism;

a second memory controller that controls access to a second system memory; and

wherein said first memory controller speculatively continues to energize said Row Address Strobe for said selected row based upon historical information recorded by said second memory controller.

2. (previously presented) The data processing system of Claim 1, wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip.

3. (previously presented) The data processing system of Claim 1, wherein said access history mechanism maintains a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

4. (previously presented) The data processing system of Claim 1, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said access history mechanism stores said historical information on a per-bank basis.

5. (previously presented) The data processing system of Claim 1, wherein said plurality of rows are organized in one or more banks, and wherein said memory controller speculatively continues to energize said Row Address Strobe for said selected row until a next access to another row within a same bank as said selected row.

6. (cancelled)

7. (currently amended) ~~The~~ A data processing system ~~of Claim 1~~, comprising:

one or more processing cores;

a memory controller, coupled to said one or more processing cores, that controls access to a system memory containing a plurality of rows organized in one or more banks, said memory controller having an access history mechanism that maintains historical information regarding prior memory accesses, wherein said memory controller, responsive to a memory access request, directs an access to a selected row among the plurality of rows in the system memory to service the memory access request and speculatively causes the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism; and

~~wherein said plurality of rows are organized in one or more banks, and wherein said data processing system further comprises:~~

~~a system interconnect coupling said plurality of processing cores; and~~

one or more cache hierarchies coupled to said plurality of processing cores and to said memory controller, wherein said one or more cache hierarchies ~~that~~ cache data retrieved from said system memory~~, wherein said one or more cache memories~~ and communicate historical bank access information to said memory controller, said historical bank access information communicated to said memory controller including historical bank access information of

memory access requests serviced by said one or more cache hierarchies rather than said memory controller.

8. (currently amended) A memory controller for controlling a system memory of a data processing system including another memory controller, wherein the system memory includes a plurality of rows, said memory controller comprising:

an access history mechanism that maintains historical information regarding prior memory accesses; and

a state machine that, responsive to a memory access request, directs an access to a selected row among the plurality of rows in the system memory to service the memory access request and speculatively causes the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism, wherein said memory controller speculatively continues to energize said Row Address Strobe for said selected row based upon historical information recorded by said another memory controller..

9. (previously presented) The memory controller of Claim 8, wherein said access history mechanism maintains a respective memory access history for each of a plurality of threads executing within said data processing system.

10. (previously presented) The memory controller of Claim 8, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said access history mechanism stores said historical information on a per-bank basis.

11. (previously presented) The memory controller of Claim 8, wherein said plurality of rows are organized in one or more banks, and wherein said state machine causes said system memory to

speculatively continue to energize said Row Address Strobe for said selected row until a next access to another row within a same bank as said selected row.

12. (canceled)

13. (currently amended) A method of operating a memory controller of a system memory of a data processing system, wherein the system memory contains a plurality of rows, said method comprising:

said memory controller maintaining historical information regarding prior memory accesses with an access history mechanism;

in response to receipt of a memory access request, directing an access to a selected row among the plurality of rows in the system memory to service the memory access request; and

speculatively directing the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism, wherein said step of speculatively continuing to energize said selected row comprises speculatively continuing to energize said Row Address Strobe for said selected row based upon historical information recorded by another memory controller.

14. (previously presented) The method of Claim 13, wherein said maintaining comprises maintaining a respective memory access history for each of a plurality of threads executing within said data processing system.

15. (previously presented) The method of Claim 13, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said maintaining comprises maintaining said historical information of said access history mechanism on a per-bank basis.

16. (previously presented) The method of Claim 13, wherein said plurality of rows are organized in one or more banks, and wherein said step of speculatively continuing to energize said selected

row comprises speculatively continuing to energize said Row Address Strobe for said selected row until a next access to another row within a same bank as said selected row.

17. (canceled)

18. (previously presented) The data processing system of Claim 1, wherein said access history mechanism comprises one or more state machines each having a plurality of different states, wherein each of said plurality of different states represents a prediction regarding whether the system memory should continue to energize a Row Address Strobe of said selected row of said system memory following an access.

19. (previously presented) The memory controller of Claim 8, wherein said access history mechanism comprises one or more state machines each having a plurality of different states, wherein each of said plurality of different states represents a prediction regarding whether the system memory should continue to energize a Row Address Strobe of said selected row of said system memory following an access.

20. (previously presented) The method of Claim 13, wherein said maintaining comprises maintaining one or more state machines each having a plurality of different states, wherein each of said plurality of different states represents a prediction regarding whether the system memory should continue to energize a Row Address Strobe of said selected row of said system memory following an access.